IDEC Chip Design Contest

Layout-Aware Area Optimization of 10T-Based Content Addressable Memory (CAM)

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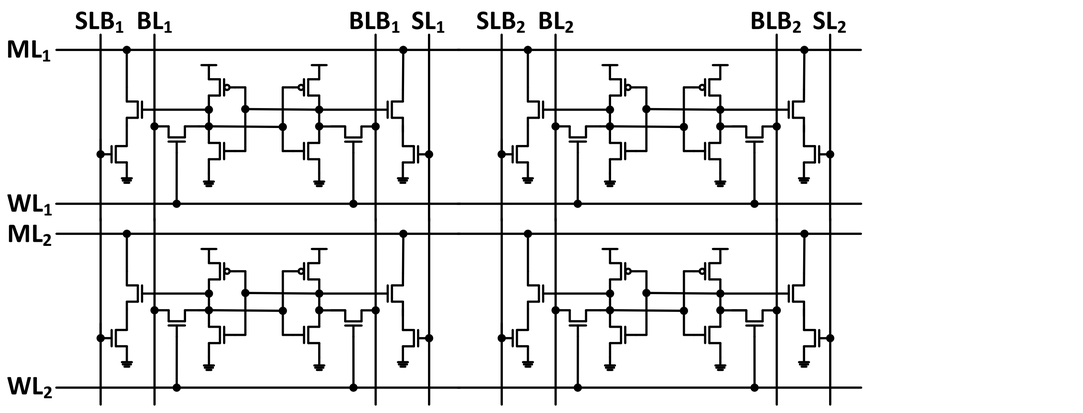
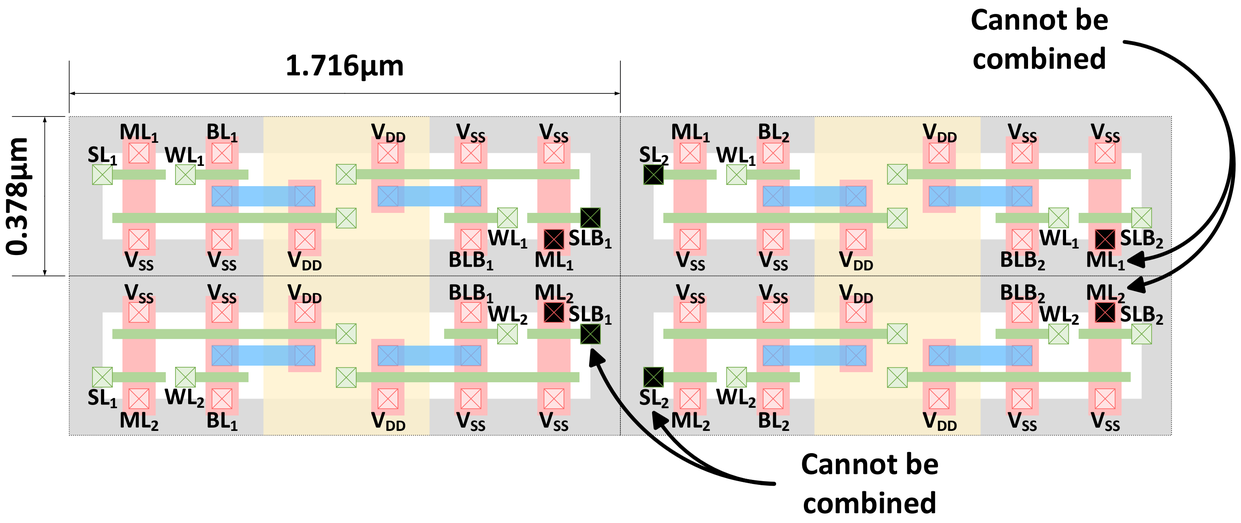
▪ MOTIVATION

- **Binary-CAM**, based on a 6T-SRAM bit-cell, requires dedicated search lines and match lines for each cell which cause higher area and power overhead than conventional location-addressed memories.
- Conventional BCAM layouts has non-shareable search-line (SL) contacts and non-shareable match-line (ML) contacts.
- A new layout with sharing word-line (WL) contacts and power/ground contacts between adjacent cells is proposed, reduces routing redundancy and shrinks the cell footprint.



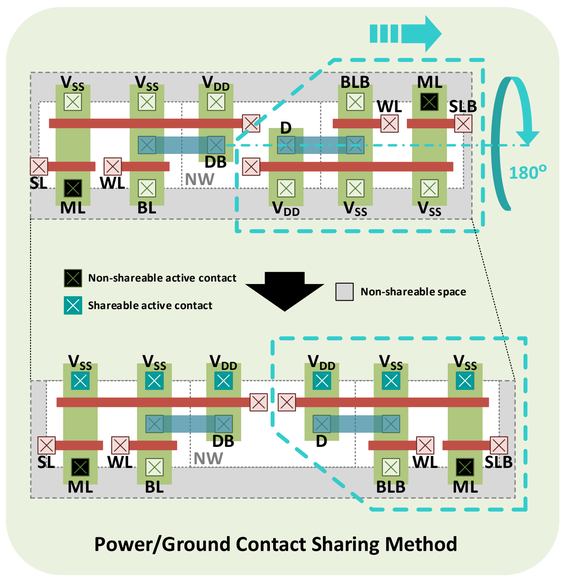


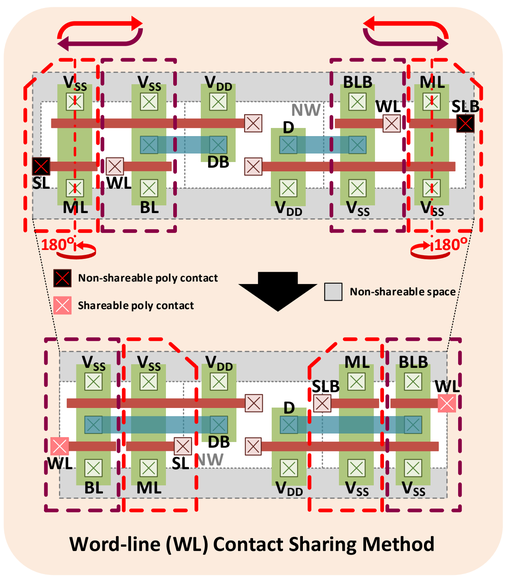
<Conventional 2 × 2 CAM Schematic and Layout >

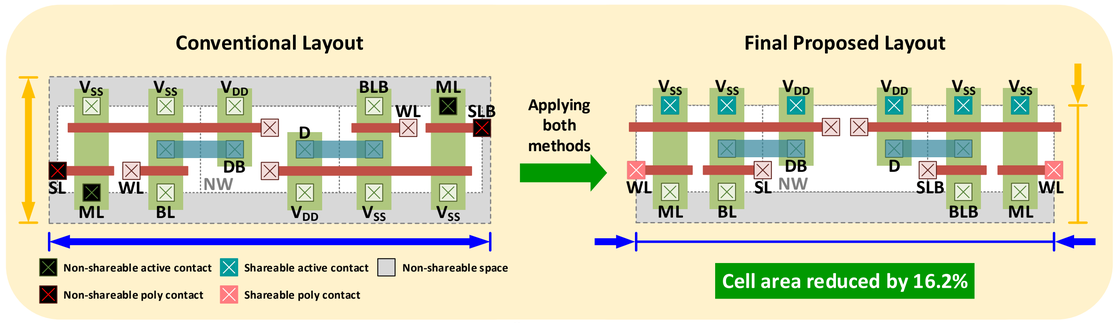
▪ BNN-CAM ARRAY

- Unlike RAM, CAM enables parallel search within one cycle by using a two-layer stacked NMOS structure beside the bit cell.
- When the search data differs from the stored data, one stacked NMOS transistor turns on, forming a pull-down path that discharges the ML.
- When the search data matches the stored data, both NMOS transistors remain off, so no current path is formed from the match line to ground.
- However, CAM requires four additional transistors and independent match/search-line contacts, increasing routing complexity, area, and reducing density compared to RAM.

▪ LAYOUT MODIFICATION TECHNIQUE

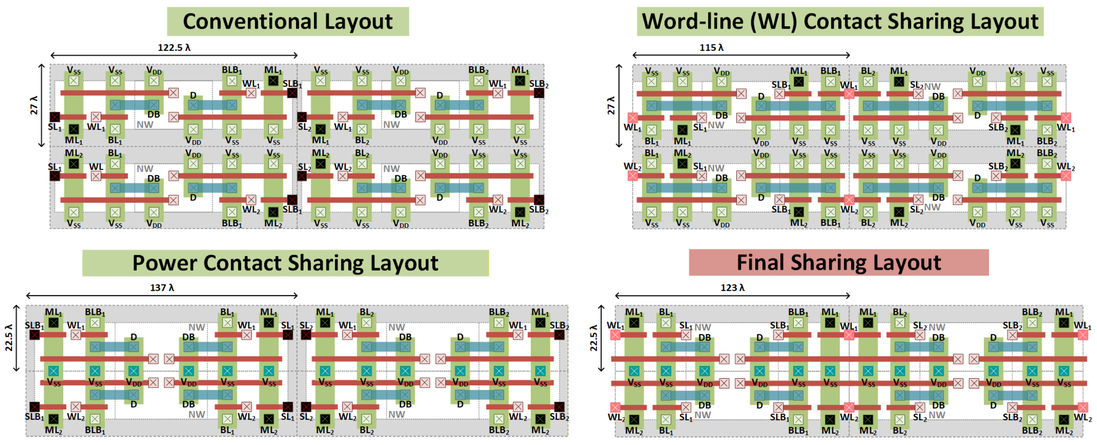






<Implementation of Power/Ground Contact Sharing Method and Word-line (WL) Contact Sharing Method>

▪ RESULTS

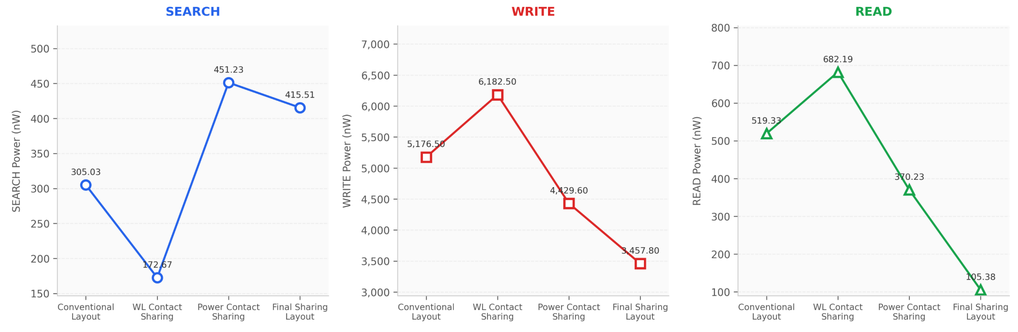


< 2 × 2 CAM Layout Visualization for All Designs>

AREA AND POWER COMPARISON TABLE FOR EACH LAYOUT

Layout	Bitcell Area (µm²)	Search Op. (nW)	Write Op. (nW)	Read Op. (nW)
Conventional	0.6486	305.03	5176.5	519.33
Word-line (WL) Contact Sharing	0.6054 (-6.66 %)	172.67	6182.5	682.19
Power Contact Sharing	0.6093 (-6.06 %)	451.23	4429.6	370.23
Final Sharing	**0.5437 (-16.17 %)**	415.51	3457.8	105.38

POWER CONSUMPTION COMPARISON ACROSS LAYOUT DESIGNS



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